WBS 6.4
Liquid Argon Calorimeter System
Technical Overview

John Parsons
US ATLAS HL-LHC Level-2 Manager for the LAr Calorimeter System
Columbia University

NSF Conceptual Design Review of the U.S. ATLAS HL-LHC Upgrade
National Science Foundation
Arlington, VA
March 8 - 10, 2016

Bio Sketch of Level-2 Manager

John Parsons (Professor of Physics, Columbia University)

- ATLAS roles include:
    - Team Leader of Columbia University ATLAS group, since we joined as one of the original US groups to join the LHC (in 1995)
    - Since 4/2010, US ATLAS Level-2 Manager for LAr Maintenance & Operations
    - Leader of group that developed and produced the Front End Board (FEB) of the current LAr calorimeter readout, as well as 5 custom ASICs
    - During original ATLAS construction, served for 5 years ('03 – '08) as :
        - Member of ~20-person ATLAS Executive Board and ~30-person ATLAS Technical Management Board
        - LAr Electronics Coordinator
        - Member of ~10-person LAr Management Group and ~20-person LAr Steering Group
    - Served for 6 yrs ('97 – '03) as Co-Convenor of ATLAS Top Quark physics working group, and as member of ~20-person ATLAS Physics Coordination Board

- Previous experiments (and hardware roles) include:
    - DZero ('00 – '10, LAr trigger electronics), SSC ('91 – '93, Leader of GEM LAr electronics), ZEUS ('90 – '99, Calorimeter readout electronics), ARGUS ('85 – '90, Microvtx detector)

- Education/Outreach, Other:
    - PI of Nevis Labs REU Site since inception in 2001, Founder of Science-on-Hudson public lecture series, Columbia U. Committee on Science Instruction, …
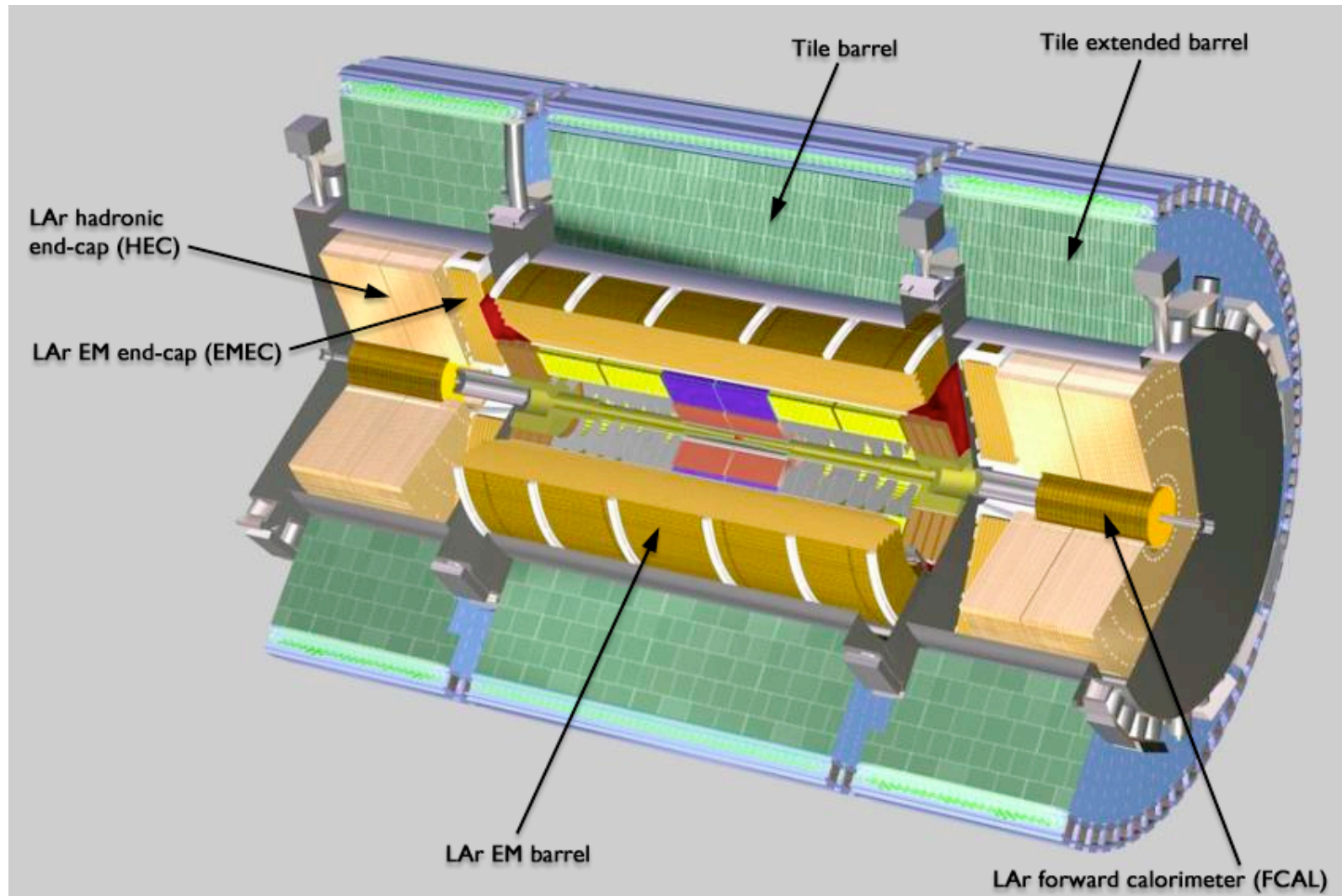   - APS Fellow

Outline

- **System Overview and Upgrade Motivation**
    - Current LAr Calorimeter System
    - Physics Motivations and Flow-down to Technical Requirements
    - ATLAS Upgrade Plans
- **Proposed NSF HL-LHC Upgrade Scope**
    - Work Breakdown Structure and Contributing Universities
    - U.S. Deliverables
- **Ongoing R&D Efforts**
- **(Brief Overview of) Construction Project Management**
    - Construction Project Budget and Schedule
    - Risk, Contingency, and Quality Assurance
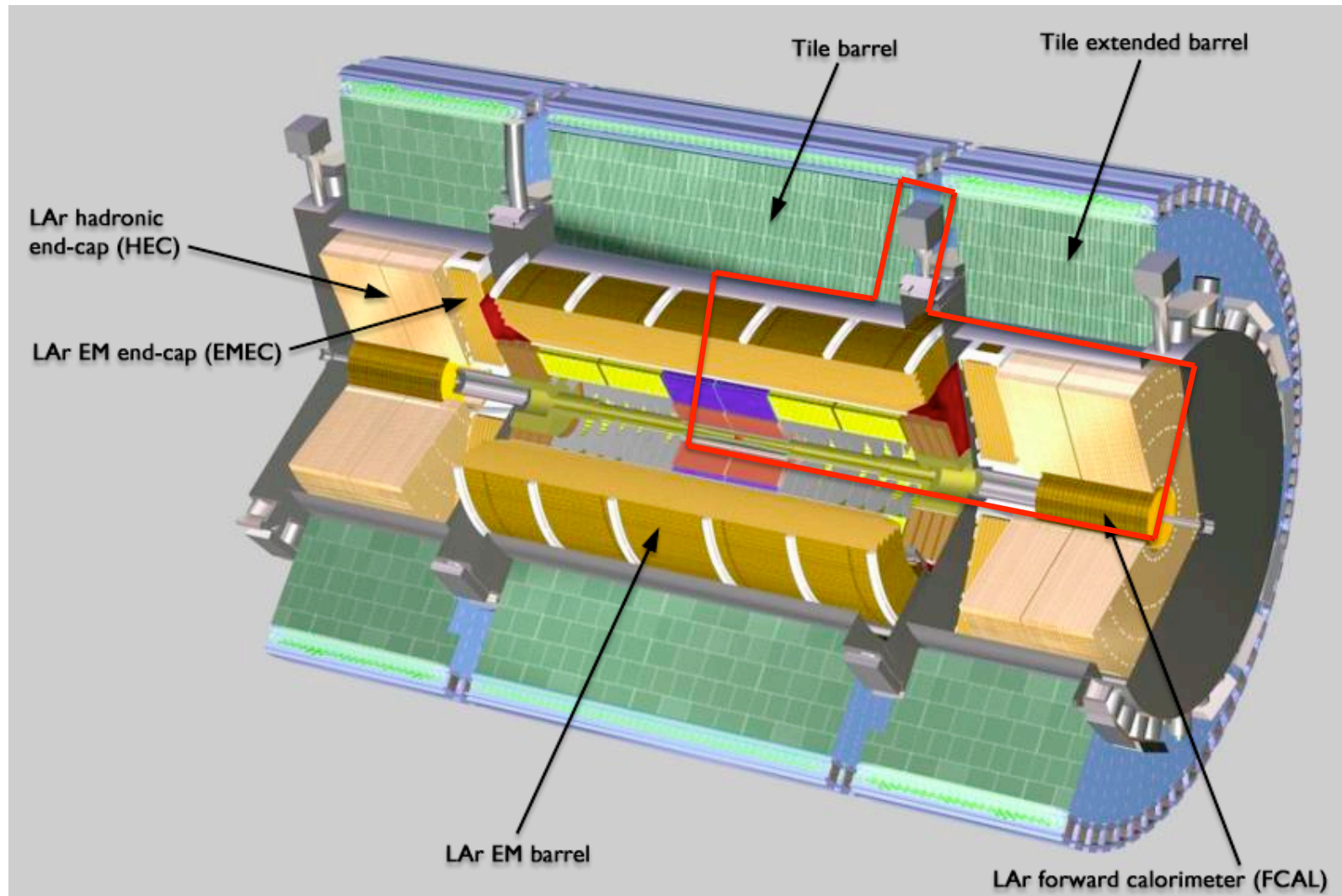- **Closing Remarks**

ATLAS Calorimeter System

ATLAS Calorimeter System

Tile barrel

Tile extended barrel

LAr hadronic end-cap (HEC)

LAr EM end-cap (EMEC)
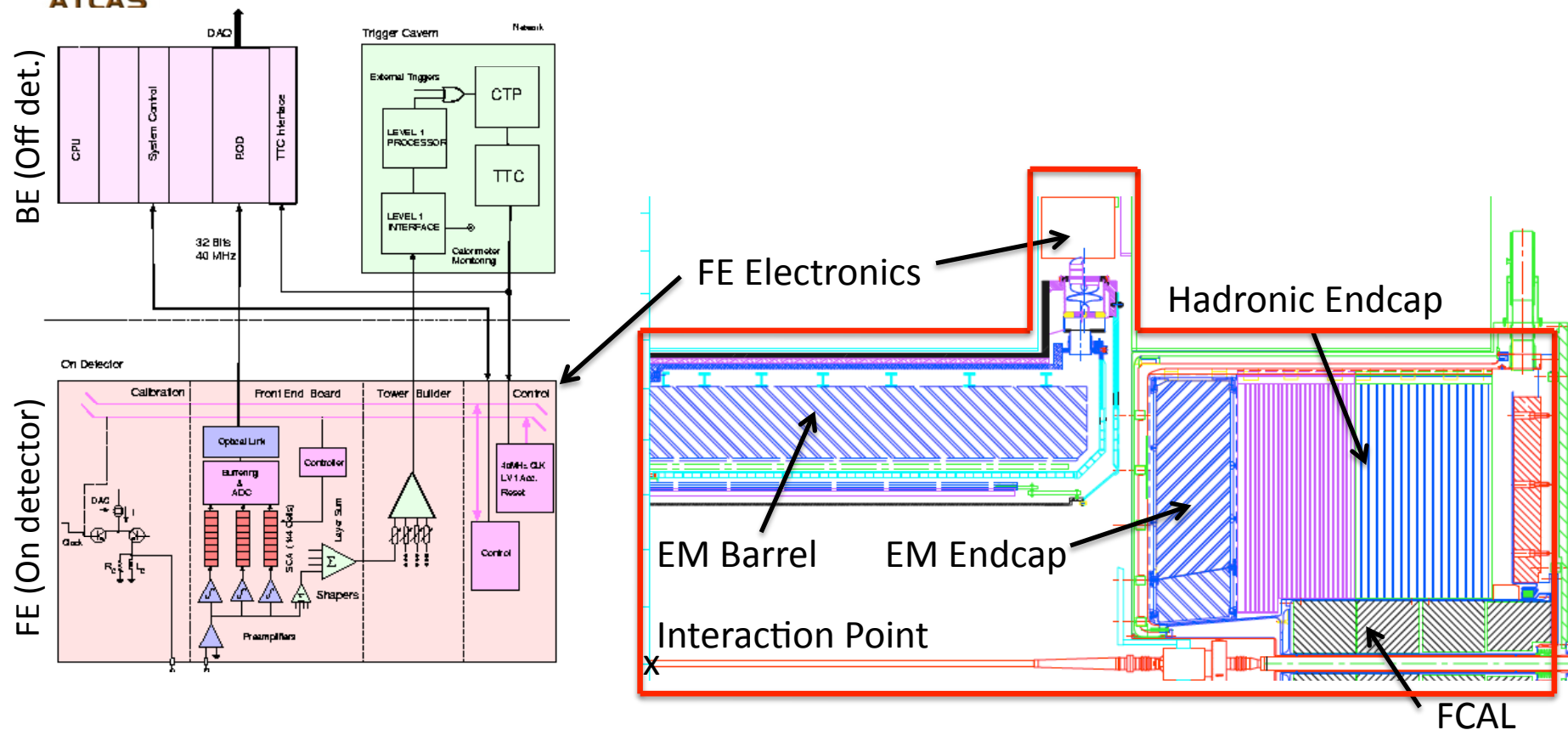
LAr EM barrel

LAr forward calorimeter (FCAL)

LAr Calorimeter System

LAr Calorimeter System

- In Phase I, upgrading L1 trigger electronics to be able to cope with lumi of 2E34

FE Electronics

Hadronic Endcap

EM Barrel   EM Endcap

Interaction Point

FCAL

LAr Calorimeter System

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FCAL
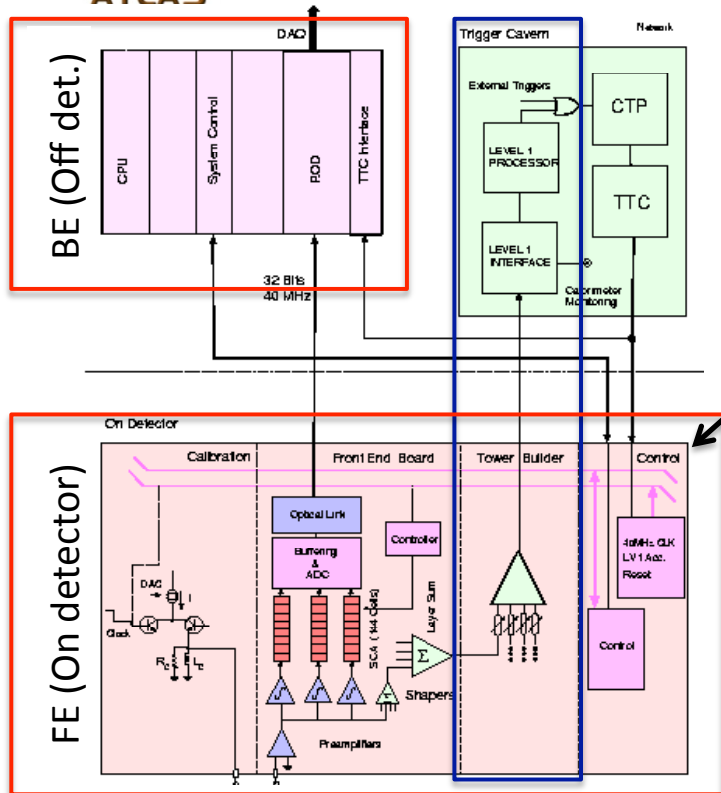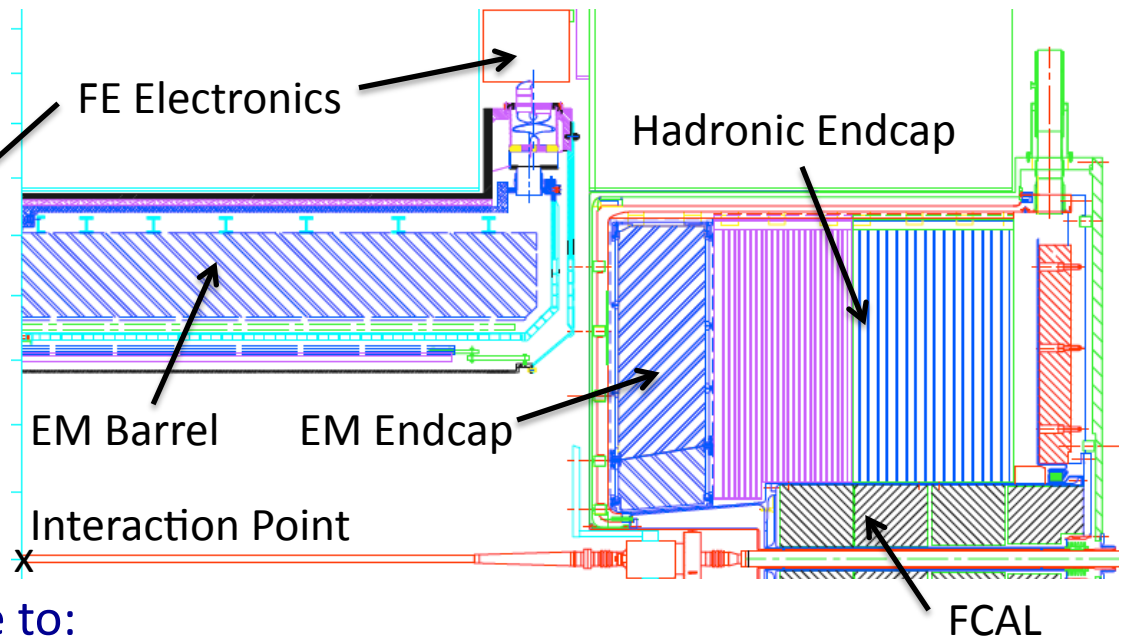
- LAr HL-LHC upgrade plans are to:
  - Replace LAr readout electronics, both front-end (FE) and back-end (BE)
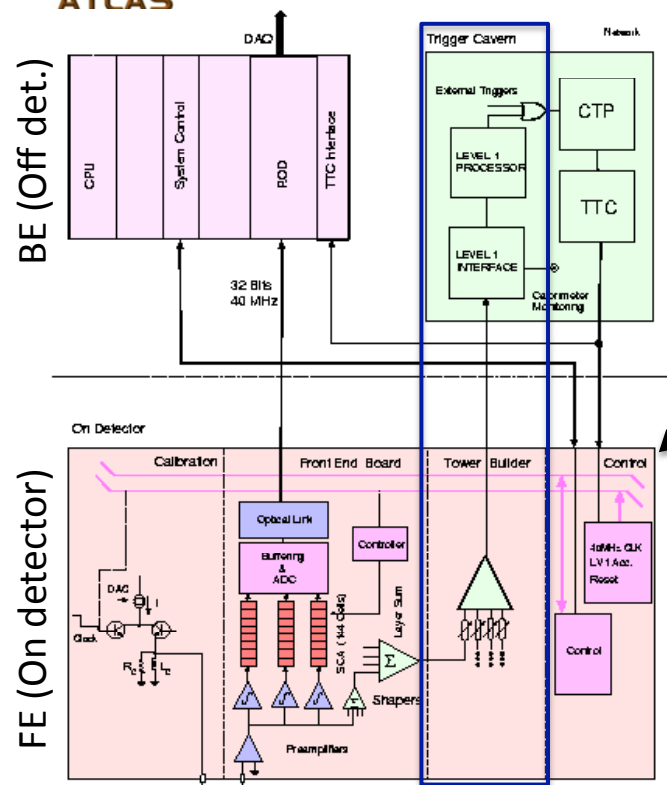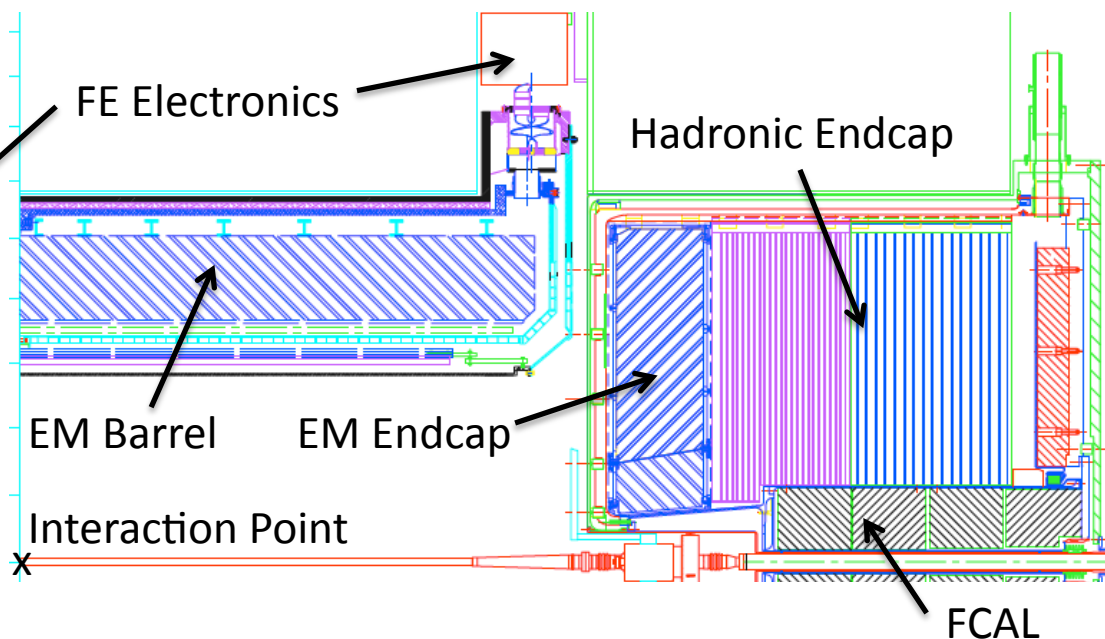
LAr Calorimeter System

- In Phase I, upgrading L1 trigger electronics to be able to cope with lumi of 2E34

HGTD

sFCAL

- LAr HL-LHC upgrade plans are to:

Scope Opportunity

- Replace LAr readout electronics, both front-end (FE) and back-end (BE)
- Possibly modify the forward region, with options including
  - Possible new sFCAL to replace FCAL (or possible MiniFCAL in front of FCAL)
  - Possible high-granularity timing detector (HGTD) in front of endcap cryostat

Physics → NSF Scope Flowdown

SCIENCE GOALS	SCIENCE REQUIREMENTS	NSF SCOPE
$H \to 4\mu$ (2.2%) VBF $H \to ZZ^*, WW^*$ (17%,14%) VBS ssWW (5.9%) SUSY $\chi_1^\pm \chi_2^0 \to \ell bb + X$ (850 GeV)	**Muon Trigger** • single μ p_T threshold ~ 20 GeV • geometric accept: 95% (barrel)	• Muon Electronics • Tile Electronics • sMDT • L0Muon
VBF $H \to ZZ^*, WW^*$ (17%,14%) VBS ssWW (5.9%) SUSY $\chi_1^\pm \chi_2^0 \to \ell bb + X$ (850 GeV)	**Electron Trigger** • single e p_T threshold ~ 22 GeV	• LAr+Tile Electronics • L1Global • L1Track/FTK++
$HH \to 4b$ (4.4σ KK Graviton)	**Jet Triggers** • 4-jet E_T threshold ~ 75 GeV • "fat" jet threshold ~ 375 GeV • jet-vertex confirmation at L1	• LAr+Tile Electronics • L1Global • L1Track/FTK++
Compressed SUSY ($\chi_1^\pm \chi_2^0$)	**Missing E_T Trigger** • ME_T threshold ~ 200 GeV • track-based ME_T correction	• LAr+Tile Electronics • L1Global • L1Track/FTK++

Cost-Effective Trigger System that meets Science Requirements:
• <L0 accept>=1 MHz (6/10μs); <L1 accept>=400 kHz (30/60μs); <to storage>=10 kHz

Physics → NSF Scope Flowdown

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Compressed SUSY ($\chi_1^\pm \chi_2^0$)

SCIENCE REQUIREMENTS

Muon Trigger
- single μ p_T threshold ~ 20 GeV
- geometric accept: 95% (barrel)

Electron Trigger
- single e p_T threshold ~ 22 GeV

Jet Triggers
- 4-jet E_T threshold ~ 75 GeV
- "fat" jet threshold ~ 375 GeV
- jet-vertex confirmation at L1

Missing E_T Trigger
- ME_T threshold ~ 200 GeV
- track-based ME_T correction

NSF SCOPE

- Muon Electronics
- Tile Electronics
- sMDT
- L0Muon

- LAr+Tile Electronics
- L1Global
- L1Track/FTK++

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Cost-Effective Trigger System that meets Science Requirements:
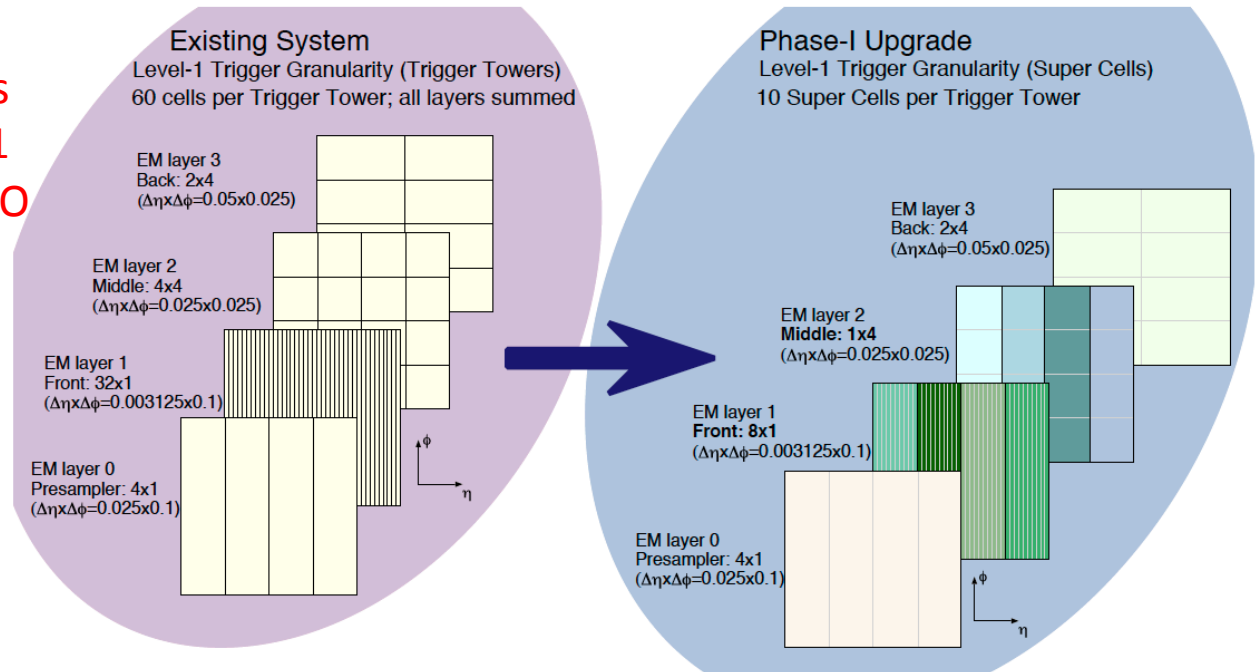- <L0 accept>=1 MHz (6/10µs); <L1 accept>=400 kHz (30/60µs); <to storage>=10 kHz

LAr HL-LHC Upgrade Motivation

- Meeting HL-LHC physics goals requires maintaining ability to trigger on low pT objects (eg. ~20 GeV electrons and photons) in HL-LHC environment
  - These EM triggers are dominated by fakes from jets, and their rates rise quickly with instantaneous luminosity (eg. 22 GeV single electron trigger using the Phase I trigger scheme would give a L1 trigger rate of 200 kHz at HL-LHC luminosity of 7.5E34)

- The existing LAr readout and trigger satisfies the original ATLAS detector specifications, including L1 trigger rate < 100 kHz, L1 latency < 2.5 µs, …
  - This performance is NOT adequate to achieve the HL-LHC physics goals

- To achieve HL-LHC physics goals, move to new HL-LHC TDAQ architecture, including L0/L1 trigger rates up to 1 MHz/400 kHz, with latencies up to 10 µs/60 µs
  - To adopt new TDAQ, we MUST completely replace LAr readout electronics (both FE and BE)
  - To be able to keep trigger thresholds low, need to provide more information at earlier trigger levels (eg. use EM shower shape variables at L1)
    - To make this possible, develop new FE electronics, implementing digitization and readout of FULL granularity (~170k channels, with ~16 bit dynamic range) at 40 MHz
    - Also need to develop new BE electronics to process this data stream, and provide inputs (for L1 and higher triggers, as well as final readout) to HL-LHC TDAQ system

LAr HL-LHC Upgrade Motivation (cont'd)

- Current L1 trigger uses analog sums of 60 LAr cells to make $\Delta\eta \times \Delta\Phi = 0.1\times0.1$ trigger towers (TT), with NO longitudinal segmentation

- Phase I upgrade will improve L1 granularity to give analog sums corresponding to 10 "super-cells" per TT

- HL-LHC will provide full granularity (6X as many channels), and with full dynamic range and full precision for each channel

Existing System
Level-1 Trigger Granularity (Trigger Towers)
60 cells per Trigger Tower; all layers summed

EM layer 3 Back: 2x4 ($\Delta\eta \times \Delta\phi = 0.05\times0.025$)
EM layer 2 Middle: 4x4 ($\Delta\eta \times \Delta\phi = 0.025\times0.025$)
EM layer 1 Front: 32x1 ($\Delta\eta \times \Delta\phi = 0.003125\times0.1$)
EM layer 0 Presampler: 4x1 ($\Delta\eta \times \Delta\phi = 0.025\times0.1$)

Phase-I Upgrade
Level-1 Trigger Granularity (Super Cells)
10 Super Cells per Trigger Tower

EM layer 3 Back: 2x4 ($\Delta\eta \times \Delta\phi = 0.05\times0.025$)
EM layer 2 Middle: 1x4 ($\Delta\eta \times \Delta\phi = 0.025\times0.025$)
EM layer 1 Front: 8x1 ($\Delta\eta \times \Delta\phi = 0.003125\times0.1$)
EM layer 0 Presampler: 4x1 ($\Delta\eta \times \Delta\phi = 0.025\times0.1$)

Layer		Elementary Cell $\Delta\eta \times \Delta\phi$	Trigger Tower $n_\eta \times n_\phi$	Trigger Tower $\Delta\eta \times \Delta\phi$	Super Cell $n_\eta \times n_\phi$	Super Cell $\Delta\eta \times \Delta\phi$
0	Presampler	0.025×0.1	4×1		4×1	0.1×0.1
1	Front	0.003125×0.1	32×1	0.1×0.1	8×1	0.025×0.1
2	Middle	0.025×0.025	4×4		1×4	0.025×0.1
3	Back	0.05×0.025	2×4		2×4	0.1×0.1

HL-LHC LAr Readout Architecture
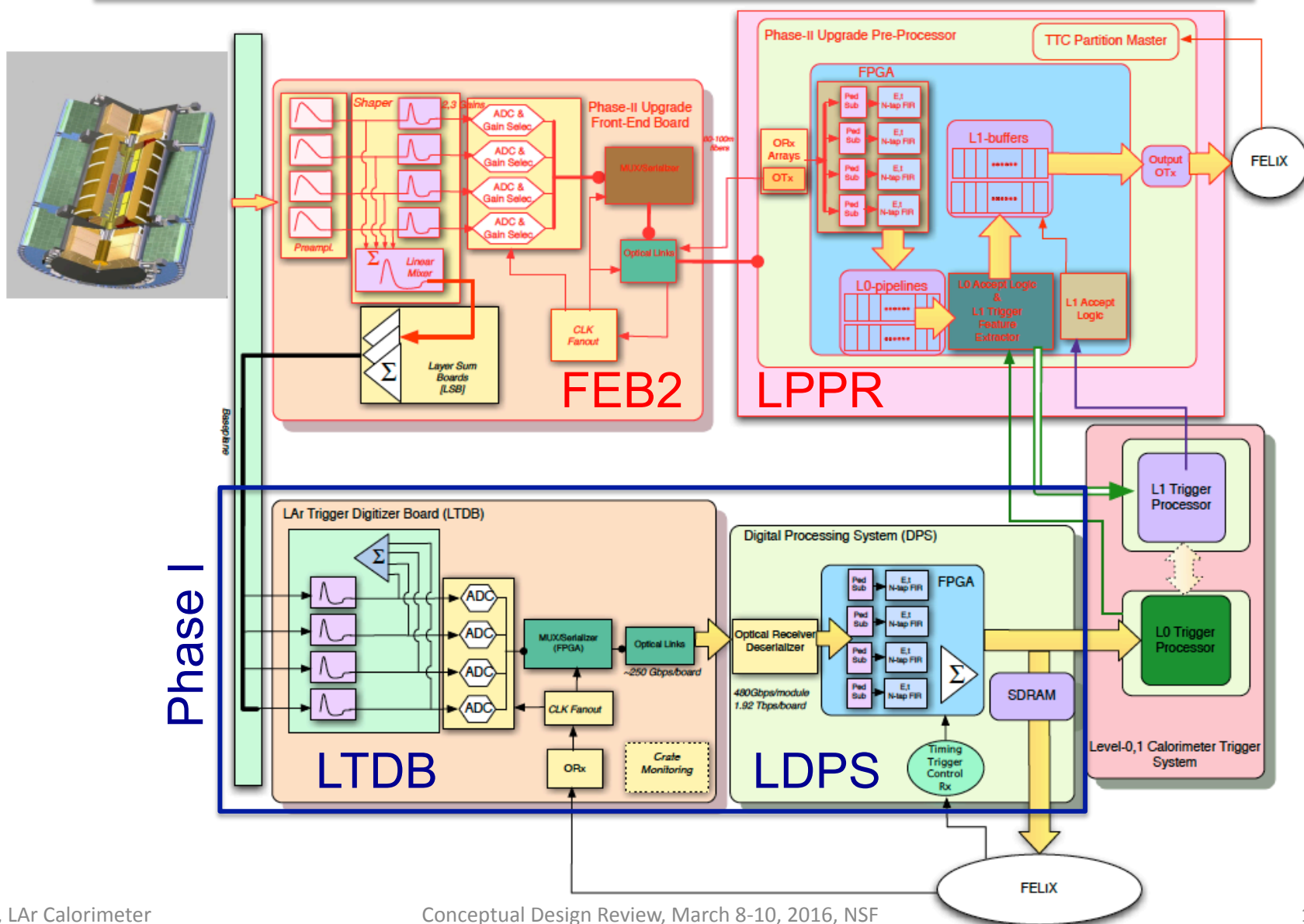
US LAr WBS Structure and Institutions

6.4 Liquid Argon WBS (NSF)	
Deliverable/Item	**Institution**
FE Electronics	
6.4.1.1 FE Electronics	Columbia (John Parsons)
6.4.2.1 FE Electronics	UT Austin (Tim Andeen)
Optics	
6.4.3.2 Optics	SMU (Jingbo Ye)
BE Electronics	
6.4.4.3 BE Electronics	Stony Brook (John Hobbs)
6.4.5.3 BE Electronics	U Arizona (Ken Johns)

- NSF deliverables organized into 3 BOEs, including efforts by 5 university groups

- DOE scope includes PA/shaper ASIC and System Integration

# NSF Fractions

NSF FRACTIONS OF HL-LHC LAR CAL UPGRADE

ATLAS WBS	ATLAS Item (Scoping Doc)	US WBS	Deliverable	NSF Fraction Design	Production
3	LAr Calorimeter	6.4	LAr Calo.		~ 22%
3.1	LAr Readout Electronics				
3.1.1	LAr FE Electronics				~ 29%
3.1.1.1	Frontend Boards (FEB2)	6.4.x.1, 6.4.x.2		100%	67%
3.1.1.2	Optical fibres and fibre plant			-	-
3.1.1.3	Frontend power dist. system			-	-
3.1.1.4	HEC LVPS			-	-
3.1.1.5	Calibration system			-	-
3.1.1.6	Shipping and logistics			-	-
3.1.2	LAr BE Electronics				~ 13%
3.1.2.1	LAr Preprocessor boards (LPPR)				
	LPPR Motherboards	6.4.x.3		100%	67%
	LPPR Mezzanines			-	-
3.1.2.2	Transition modules			-	-
3.1.2.3	ATCA shelves			-	-
3.1.2.4	ATCA switches			-	-
3.1.2.5	Server PC			-	-
3.1.2.6	Controller PC			-	-
3.1.2.7	FELIX/TTC system			-	-

- Focus our efforts on critical elements, where we can leverage our expertise and play a leadership role

HL-LHC LAr FE Electronics

- As in original construction, US groups proposing to take lead responsibility for electronics in LAr FE readout path, with deliverables including:

  - Radiation-tolerant (65 nm) ASICs
    - o Preamp/shaper (BNL, U Penn)
    - o 40 MHz ADC (Columbia)
    - o 10 Gbps Serializer (SMU)
    - o VCSEL array driver (SMU)

  - Optical transmitter (OTx) (SMU)
  - Frontend Board (FEB2) (Columbia)

- WBS items: **6.4.x.1 (FE Electronics)**, **6.4.x.2 (Optics)**, **6.4.x.5 (PA/shaper - DOE)**

- Apart from complementary French effort on Preamp/shaper, no non-US groups are currently working on these tasks

- Full system of ~170k channels requires 1524 FEB2 boards (128 channels each)

  - As in original construction, planning to produce total of 1627
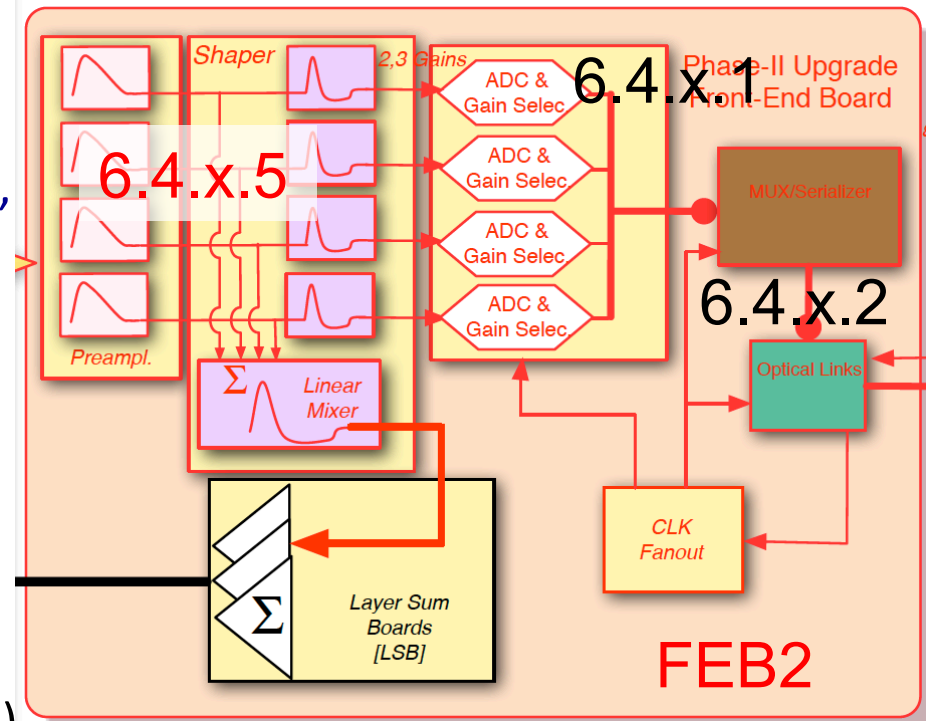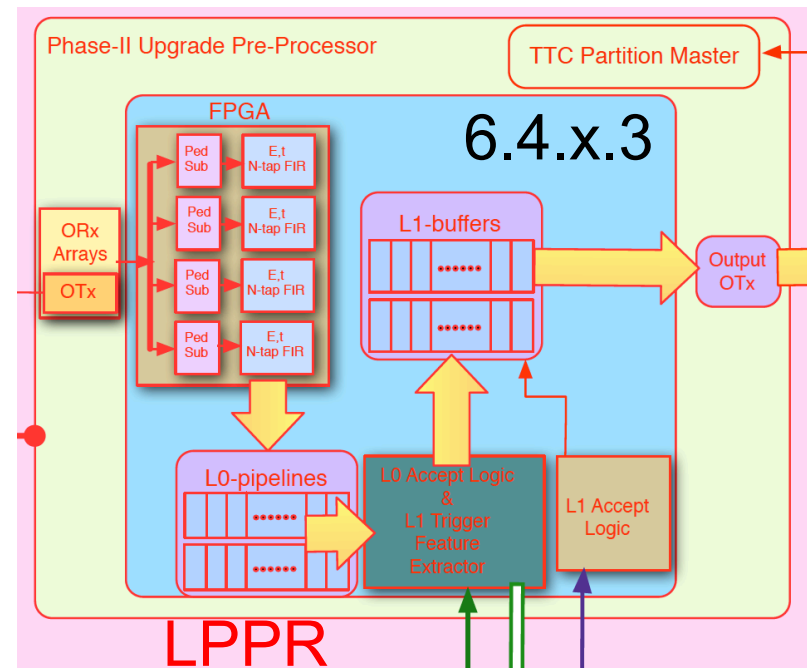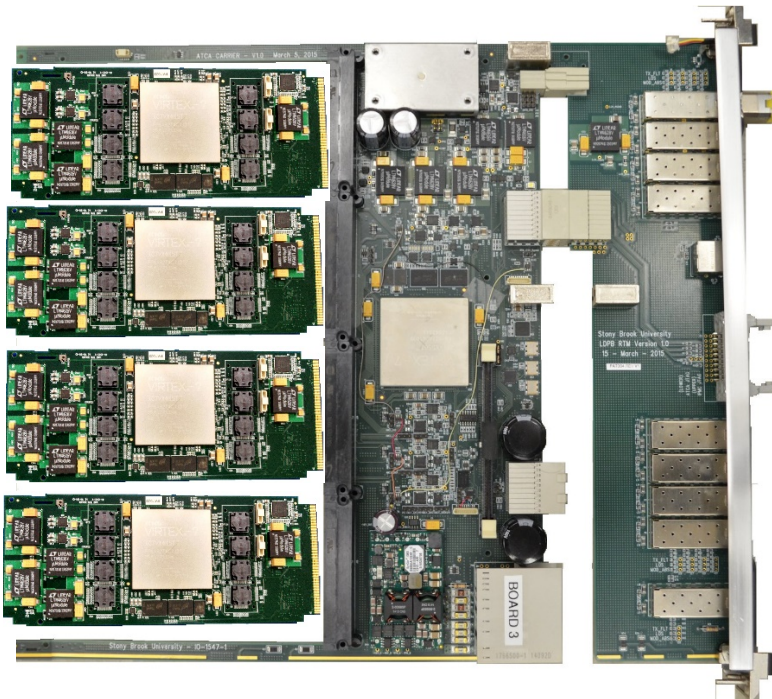
HL-LHC LAr FE Electronics

- NSF scope includes playing the leading role in development of the FE electronics for the HL-LHC, and leverages the expertise of the university groups involved

- WBS 6.4.x.1 (FE Electronics)
  - Columbia – development of FEB2, custom dual-range 12-bit 40 MHz ADC
    - o Developed original FEB, as well as 5 out of 11 custom ASICs
    - o Developed custom rad-tol 12-bit 40 MHz ADC for Phase I upgrade
  - UT Austin – ASIC testing/validation, including radiation qualification
    - o Tim Andeen (as Columbia postdoc) led Phase I ADC testing effort

- WBS 6.4.x.2 (Optical links)
  - SMU – development of 10 Gbps optical links, incl. Serializer ASIC
    - o Was responsible for optical links (1.6 Gbps) of original FEB
    - o Developing 5 Gbps Serializer ASIC + optical links for Phase I upgrade

- LPPR of HL-LHC is natural "evolution" of ATCA-based Phase I LDPS, developed by US groups working with European groups (primarily LAPP Annecy)

Prototype LDPS

- As in Phase I, Stony Brook/UAz propose to develop LPPR motherboard (MB) (WBS 6.4.x.3), both hardware and firmware (140 MBs needed in total)

  - Stony Brook – emphasis on hardware
  - U Arizona – emphasis on associated firmware

HL-LHC LAr BE Electronics

- NSF scope includes playing the leading role in development of the BE motherboard for the HL-LHC, and leverages the expertise of the university groups involved

- WBS 6.4.4.3 (BE Electronics)
  - Stony Brook – ATCA MB (carrier) and RTM (Rear Transition Module) design, prototyping & production
    - Responsibility for Phase I back end motherboard (ATCA cutout carrier) and RTM hardware
    - Included test AMC daughter card and additional smaller testing boards

- WBS 6.4.5.3 (BE Firmware)
  - Univ. of Arizona – Firmware for ATCA MB (carrier)
    - Sole responsibility for all Phase-I motherboard firmware
   - Responsible for portions of Phase-I AMC mezzanine firmware

Research & Development

- R&D so far has focused on long-lead items, in particular custom ASIC developments, including:

  - PA/shaper (BNL with U Penn) – 65 nm CMOS, as well as SiGe as backup (aim for technology decision by time of TDR, ~ fall 2017) – DOE scope

  - ADC (Columbia, in collab. with Columbia/UT Dallas EE depts) – 65 nm CMOS

  - VCSEL driver and Serializer (SMU) – 65 nm CMOS

- In addition, some R&D funding has been used to support ongoing (s)FCAL studies

- More details on LAr R&D program and plans in next talk

NSF Schedule & Milestones

U.S. ATLAS HL-LHC Upgrade Project
WBS 6.4 Liquid Argon NSF Deliverable Summary Schedule
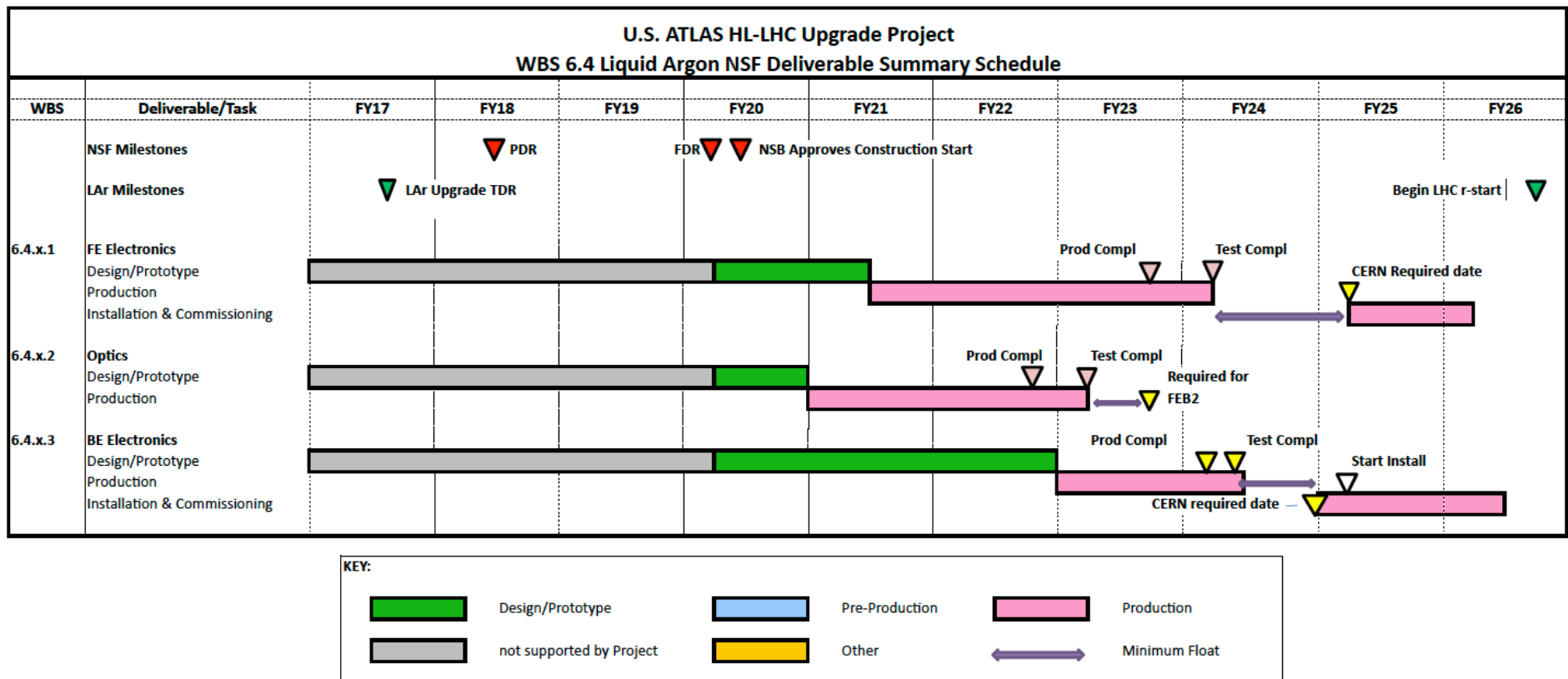
- US schedule developed to be consistent with LAr milestones presented in Scoping Document
- Planning includes 6-12 months of schedule float

6.4	Liquid Argon			
6.4.x.1	FE Electronics	Frontend Board (FEB2)	PA/shaper ASIC (BNL/UPenn - DOE scope)	Maintain tight coordination and oversight via System Engineering. Well-advanced SiGe version is a backup in case of problems with development of baseline in 65 nm CMOS. Complementary efforts underway in France.
6.4.x.2	Optics		Project self-contained in NSF scope	
6.4.x.3	BE Electronics	LPPR Motherboard (MB)	Mezzanine card (France)	Clearly define, with help from System Engineering, interfaces between MB and mezzanines. Develop mezzanine-style test cards that will allow MB to be fully tested and qualified even without final mezzanines being available.

- **Have worked to minimize potential impact of external delays**
  - FEB2 and LPPR MB production testing and validation/acceptance procedures will be clearly defined to minimize reliance on external deliverables
  - System Engineering plays important role, ensuring interfaces are properly defined, etc.
- **PA/shaper ASIC is essential component of production FEB2 boards**
  - Baseline and (well-advanced) backup developments are part of DOE scope, and will be tightly coordinated within US ATLAS
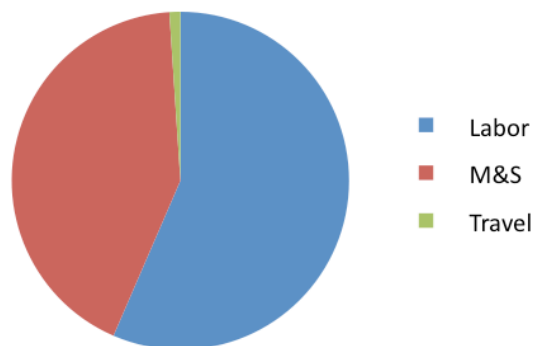 - There is also complementary development effort in France

Cost and Effort Estimates

- Cost and effort estimates for NSF scope are detailed in 3 BOEs
  - FE Electronics, Optics, BE Electronics

- Given the similarity of our HL-LHC deliverables to our previous ATLAS responsibilities, cost and manpower estimates are mostly based on our experience with either the original ATLAS construction project or the ongoing ATLAS Phase I upgrade project

- We assume cost sharing wherein US pays 67% fraction of M&S charges for FEB2 boards, OTx modules, and BE motherboards
  - However, we include 100% M&S costs for all US-led ASIC productions
  - These sharing arrangements are similar as for original ATLAS construction
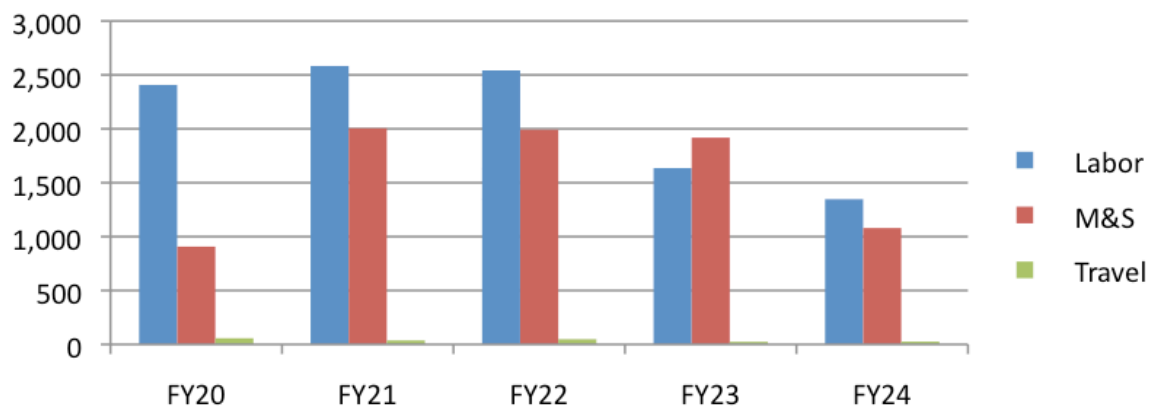
NSF Budget and Effort

6.4 Liquid Argon NSF Total Cost (AYk$)						
	FY20	**FY21**	**FY22**	**FY23**	**FY24**	**Grand Total**
NSF						
Labor	2,407	2,582	2,541	1,635	1,347	10,512
M&S	907	2,005	1,991	1,918	1,079	7,900
Travel	57	37	49	25	26	195
NSF Total	**3,371**	**4,624**	**4,581**	**3,578**	**2,453**	**18,607**

WBS 6.4 LAr NSF Resource Breakdown

WBS 6.4 LAr L2 NSF Fiscal Year Costs AYk$

NSF Cost and Effort (by Deliverable)

6.4 Liquid Argon Total NSF Cost by Deliverable (AYk$)

Deliverable/Item	FY20	FY21	FY22	FY23	FY24	Total
FE Electronics	**1,451**	**2,595**	**2,758**	**2,232**	**1,378**	**10,414**
6.4.1.1 FE Electronics	1,333	2,474	2,634	2,117	1,260	9,818
6.4.2.1 FE Electronics	119	121	123	115	118	596
Optics						
6.4.3.2 Optics	991	1,115	1,116	173	0	3,396
BE Electronics	**929**	**914**	**708**	**1,172**	**1,075**	**4,798**
6.4.4.3 BE Electronics	765	686	504	995	948	3,898
6.4.5.3 BE Electronics	164	228	204	177	126	900
NSF Grand Total	**3,371**	**4,624**	**4,581**	**3,578**	**2,453**	**18,607**

6.4 Liquid Argon NSF Total FTEs by Deliverable

Deliverable/Item	FY20	FY21	FY22	FY23	FY24	Grand Total
FE Electronics	**6.60**	**6.95**	**7.85**	**7.00**	**6.50**	**34.90**
6.4.1.1 FE Electronics	5.60	5.95	6.85	6.00	5.50	29.90
6.4.2.1 FE Electronics	1.00	1.00	1.00	1.00	1.00	5.00
Optics						
6.4.3.2 Optics	5.25	7.00	6.95	1.00	-	20.20
BE Electronics	**4.39**	**4.47**	**4.17**	**2.89**	**2.14**	**18.06**
6.4.4.3 BE Electronics	3.10	3.10	2.80	1.60	1.30	11.90
6.4.5.3 BE Electronics	1.29	1.37	1.37	1.29	0.84	6.16
NSF Grand Total	**16.24**	**18.42**	**18.97**	**10.89**	**8.64**	**73.16**

Risks

HL-LHC Upgrade Project Risk Registry for L2 Systems January 4, 2016			Risk Evaluation (L/M/H)						
WBS	Title	Risk Owner	Cost	Schedule	Scope	Contingency %	Contingency AYk$	Average Risk Score	Identified Risks (See BoEs)
6.4	**Liquid Argon**	**Parsons, John**				35%	8,792	4.5	
6.4.x.1	FE Electronics	Parsons, John	M	M	L	35%	3,645	5.0	*Problems that can only be found at bench test and system integration test may impact project schedule. *Delays in ASIC schedule can lead to assembly schedule delays. *Achieving the required performance might require additioal engineering effort. *Given preliminary nature of FEB2 design, final cost could be higher.
6.4.x.2	Optics	Parsons, John	M	L	L	35%	1,188	3.5	Delay in 1pGBT project may impact ASIC design. *Additional engineering could be effort required for ASIC. * Finding vendor qualified to assemble OTx
6.4.x.3	BE Electronics	Parsons, John	M	M	L	35%	1,840	5.0	*Problems that can only be found at bench teat and system integration test may impact project schedule. *Complexity of board requires complex manufacture and assembly process, needs more iterations. *A vendor part may require an intervention at the level of design of the overall system and some modifications of the assemblies.
6.4.x.4	System Integration	Parsons, John	M	M	L	35%	1,098	5.0	*Problems that can only be found at integration stage may impact project schedule and require modifications to one or more components. *A vendor part may require intervention at the level of design of the overall system and some modificaiotn of the assemblies.
6.4.x.5	PA/Shaper	Parsons, John	M	L	M	35%	1,021	4.5	*Problems that can only be found at bench test and system integration test may impact project schedule, requiring additional engineering work.. *Late delivery of ASICs. *Analog circuits can require multiple submissions due to unfreseen performance or manufacturing issues

DOE Scope

- Leading risks, and mitigation strategies, identified in BOEs
    - For example, cost and schedule risks in custom ASIC development, common fabrication run, …

Examples of Risks Considered

- ## WBS 6.4.x.1 – FE Electronics

  - Potential problem: Delay in any ASIC could prevent shared production run (and reduced cost due to sharing of NRE costs).

  - Mitigation: Add engineering efforts to perform extensive and comprehensive chip evaluation test, aim to solve all potential issues in early prototype runs. Use schedule contingency to keep the various ASIC productions schedules aligned. Use 65 nm CMOS process, which is used for a large number of HL-LHC ASICs, in order to be in a position to find other partners to share an additional production run if required, thereby sharing the additional costs.

- ## WBS 6.4.x.2 – Optical Links

  - Potential problem: More effort could be required in ASIC design

  - Mitigation: Use contingency to add additional engineering manpower if necessary.

- ## WBS 6.4.x.3 – BE Electronics

  - Potential problem: Technical issues such as cross-talk, coherent noise, jitter may only be discovered at the integration stage, and would most likely require modifications to one or more components.

  - Mitigation: Start integration early, at each prototype stage, including for components, and apply rigorous performance standards at all times. Add engineering efforts where needed.

Contingency

Budget Contingency

- Following rules adopted for assigning contingency at this conceptual design stage, 35% budget contingency assigned top-down to all LAr deliverables
- A risk-based bottom-up contingency analysis is being developed

Scope Contingency

- Provide less firmware effort for BE MBs (up to ~ $1M)
  - Decision up to FY22; would provide only minimal firmware to allow testing and validation of production MBs

- Cover M&S for < 67% of FEB2 boards/OTx modules/BE MBs (up to $1M)
  - Decision by FY20; would need to renegotiate (at level of overall ATLAS) final cost sharing

Scope Opportunity

- Cover M&S for > 67% of FEB2 boards/OTx modules/BE MBs (up to ~ $2.4M)
- HGTD contribution (up to ~ $5.3M)

Closing Remarks

- NSF scope deliverables for LAr follow directly from our expertise and experience from the original ATLAS construction project and the ATLAS Phase I Upgrade project

- This expertise also provides us with confidence in the budget/effort estimates, which (without contingency) total :
  - $18.6M and 73.2 FTE-years (NSF, FY20-24)

Backup Slides

LAr WBS Structure and Institutions

6.4 Liquid Argon WBS (NSF)

Deliverable/Item	Institution
FE Electronics	
6.4.1.1 FE Electronics	Columbia
6.4.2.1 FE Electronics	UT Austin
Optics	
6.4.3.2 Optics	SMU
BE Electronics	
6.4.4.3 BE Electronics	Stony Brook
6.4.5.3 BE Electronics	U Arizona

6.4 Liquid Argon WBS (DOE)

	Deliverable/Item	Institution
	System Integration	
	6.4.6.4 System Integration	BNL
	PA/Shaper	
	6.4.6.5 PA/Shaper	BNL
	6.4.7.5 PA/Shaper	U Penn
Scope Opportunity	**sFCAL**	
	6.4.5.6 sFCAL	U Arizona
	HGTD	
	6.4.7.7 HGTD	U Penn
	6.4.8.7 HGTD	UCSC
	6.4.9.7 HGTD	SLAC
	6.4.10.7 HGTD	U Iowa

- 8 university groups and 2 labs
- US deliverables organized into 7 BOEs
  - 5 in baseline (3 NSF, 2 DOE)
  - 2 in DOE "Scope Opportunity"

BOE Table: 6.4.x.1 FE Electronics

6.4.x.1 LAr FE Electronics						
WBS	**Description**	**Labor FTE**	**Labor Ayk$**	**M&S Ayk$**	**Travel Ayk$**	**TOTAL Ayk$**
6.4.x.1	**LAr FE Electronics**	**34.9**	**5,370**	**4,948**	**95**	**10,414**
	Instr. Physicists	5.6				
	Engineers	14.9				
	Techs	13.4				
	EE PhD Students	1.0				
6.4.1.1	**LArFE_Columbia**	**29.9**	**4,947**	**4,816**	**55**	**9,818**
	Instr. Physicists	5.6				
	Engineers	12.4				
	Techs	10.9				
	EE PhD Students	1.0				
6.4.2.1	**LArFE_UTAustin**	**5.0**	**423**	**133**	**40**	**596**
	Instr. Physicists	-				
	Engineers	2.5				
	Techs	2.5				
	EE PhD Students	-				

BOE Table: 6.4.x.2 Optics

6.4.3.2 LAr Optical Links						
WBS	**Description**	**Labor FTE**	**Labor Ayk$**	**M&S Ayk$**	**Travel Ayk$**	**TOTAL Ayk$**
6.4.3.2	**LAr Optical Links**	**20.2**	**2,374**	**981**	**40**	**3,396**
	Engineers	10.7				
	Techs	2.5				
	Students	7.0				

BOE Table: 6.4.x.3 BE Electronics

		Labor	Labor	M&S	Travel	TOTAL
WBS	**Description**	**FTE**	**Ayk$**	**Ayk$**	**Ayk$**	**Ayk$**
6.4.x.3	**LAr BE Electronics**	**18.1**	**2,768**	**1,971**	**60**	**4,798**
	Engineers	7.8				
	EE Postdocs	5.0				
	Techs	2.5				
	Students	2.8				
6.4.4.3	**LArBE_StonyBrook**	**11.9**	**2,001**	**1,868**	**30**	**3,898**
	Engineers	6.2				
	EE Postdocs	5.0				
	Techs	0.7				
	Students	-				
6.4.5.3	**LArFE_Arizona**	**6.2**	**767**	**103**	**30**	**900**
	Engineers	1.6				
	EE Postdocs	-				
	Techs	1.8				
	Students	2.8				

6.4.x.3 LAr BE Electronics

Table 14. Radiation tolerance criteria of the LAr electronics for operation at HL-LHC for a total luminosity of $3000\ \mathrm{fb}^{-1}$, including safety factors for background estimation, given in brackets. For COTS, an additional safety factor of 4 is included in case of production in unknown multiple lots. Furthermore, the ATLAS policy specifies annealing tests that allow reducing the enhanced low dose rate safety-factor to 1, which currently is set to 1.5 for ASICs and 5 for COTS.

	TID [kGy]		NIEL [$n_{\mathrm{eq}}/\mathrm{cm}^2$]		SEE [h/cm^2]	
ASIC	0.75	(2.25)	2.0×10^{13}	(2)	3.8×10^{12}	(2)
COTS (multiple lots)	9.9	(30)	8.2×10^{13}	(8)	1.5×10^{13}	(8)
COTS (single-lot)	2.5	(7.5)	2.0×10^{13}	(2)	3.8×10^{12}	(2)
LVPS (EMB and EMEC)	0.58	(30)	9.2×10^{12}	(8)	2.4×10^{12}	(8)
LVPS (HEC)	0.17	(2.25)	4.7×10^{12}	(2)	2.7×10^{11}	(2)

LAr Electronics CORE Costs

WBS ID	Upgrade Item	All Cost Scenarios [kCHF]
3.1	**LAr Readout Electronics**	**31,394**
3.1.1	**LAr Front-end Electronics**	**20,427**
3.1.1.1	Front-end Boards (FEB-2)	9,743
3.1.1.2	Optical fibres and fibre plant	4,306
3.1.1.3	Front-end power distribution system	3,123
3.1.1.4	HEC LVPS	622
3.1.1.5	Calibration System	2,484
3.1.1.6	Shipping and Logistics	150
3.1.2	**LAr Back-end Electronics**	**10,967**
3.1.2.1	LAr Pre-processor Boards (LPPR)	10,212
3.1.2.2	Transition modules	122
3.1.2.3	ATCA shelves	66
3.1.2.4	ATCA switches	76
3.1.2.5	Server PC	22
3.1.2.6	Controller PC	8
3.1.2.7	FELIX/TTC System	460

LAr Electronics Schedule (from SD)
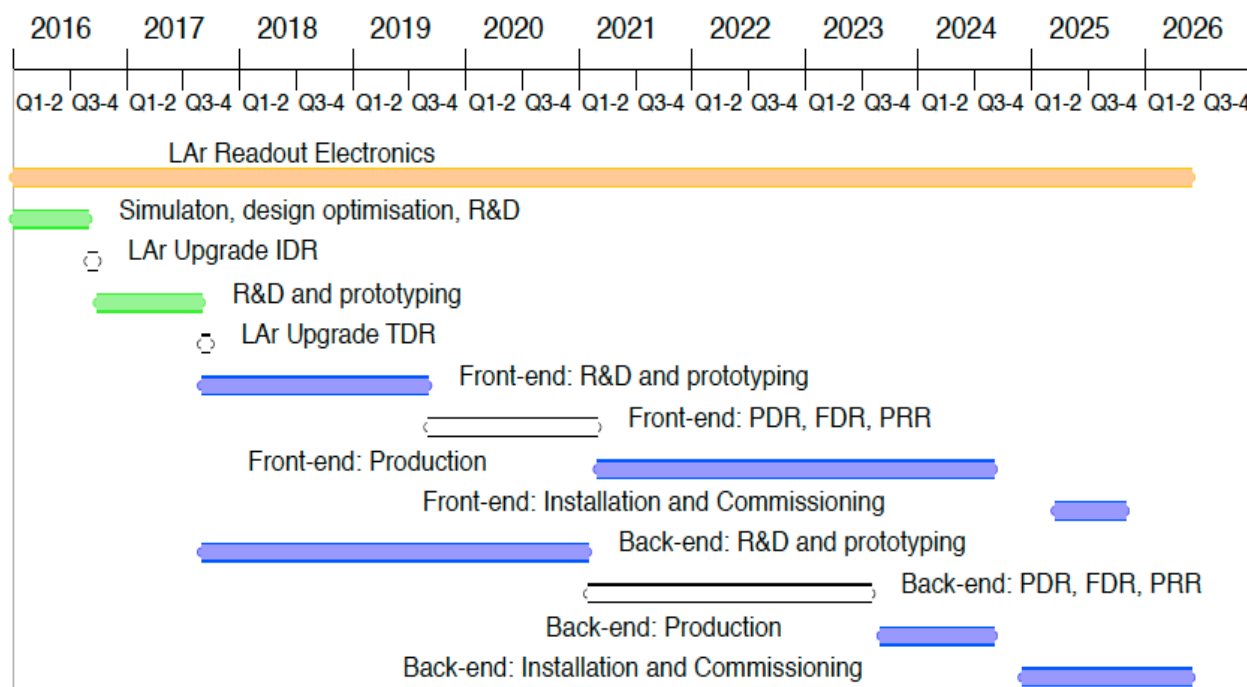
Figure 26. Overview of the time-line and milestones for the main system components of the front-end and back-end systems of the LAr readout electronics upgrade.
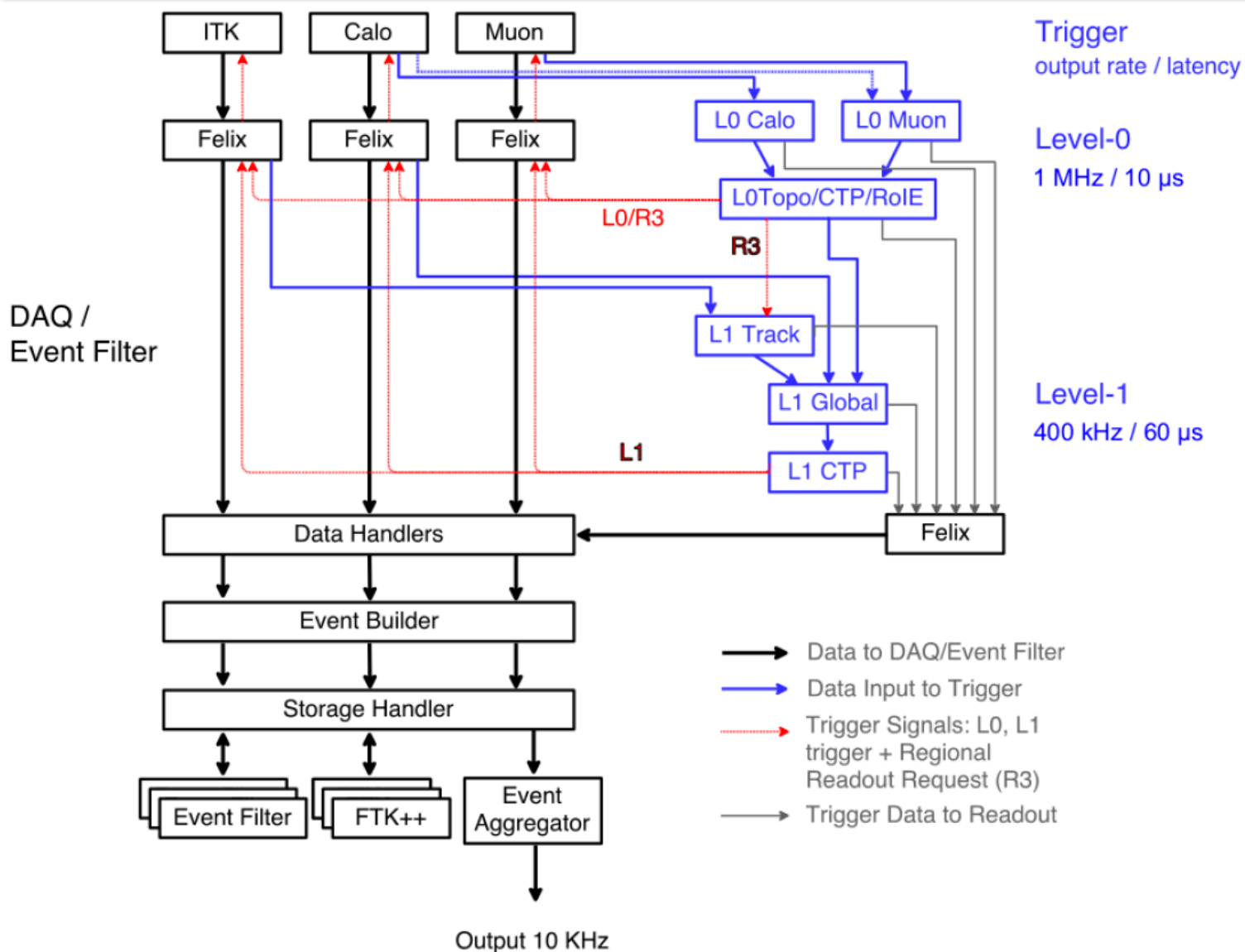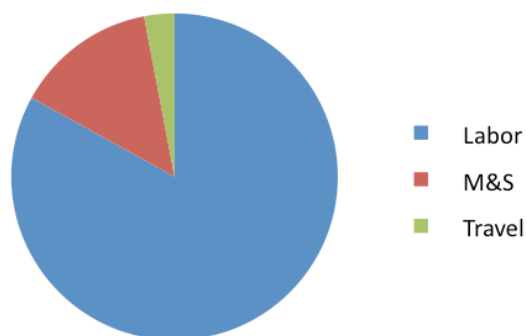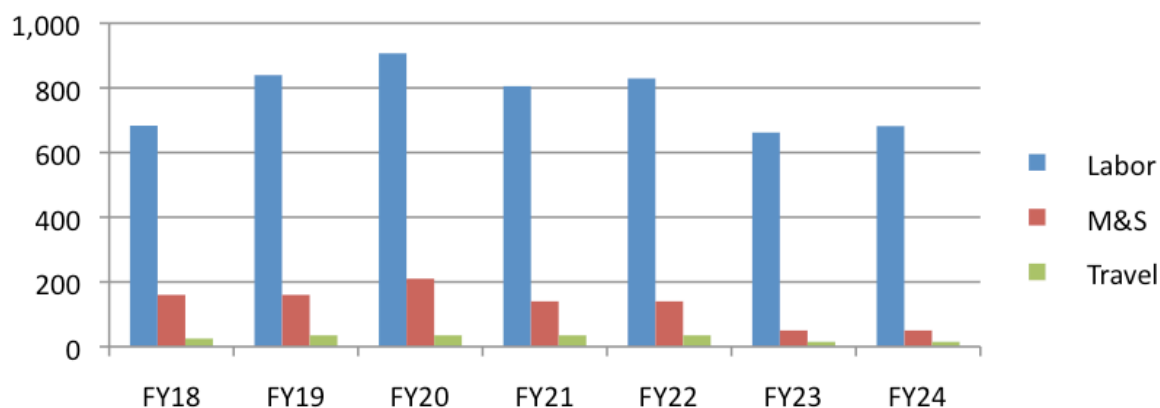
DOE Budget and Effort

6.4 Liquid Argon DOE Total Cost (AYk$)								
	FY18	FY19	FY20	FY21	FY22	FY23	FY24	Grand Total
DOE								
Labor	683	839	907	805	829	662	682	5,408
M&S	160	160	210	140	140	50	50	910
Travel	25	35	35	35	35	15	15	195
DOE Total	**868**	**1,034**	**1,152**	**980**	**1,004**	**727**	**747**	**6,513**

WBS 6.4 LAr L2 DOE Resource Breakdown

WBS 6.4 LAr L2 DOE Fiscal Year Cost AYk$

6.4 Liquid Argon Total DOE Cost by Deliverable (AYk$)

Deliverable/Item	FY18	FY19	FY20	FY21	FY22	FY23	FY24	Total
System Integration	**248**	**448**	**464**	**475**	**488**	**727**	**747**	**3,596**
6.4.6.4 System Integration	248	448	464	475	488	727	747	3,596
PA/Shaper	**621**	**586**	**688**	**505**	**516**	**0**	**0**	**2,916**
6.4.6.5 PA/Shaper	439	452	515	417	426	0	0	2,249
6.4.7.5 PA/Shaper	182	135	173	88	90	0	0	667
DOE Grand Total	**868**	**1,034**	**1,152**	**980**	**1,004**	**727**	**747**	**6,513**

6.4 Liquid Argon Total DOE FTEs by Deliverable

Deliverable/Item	FY18	FY19	FY20	FY21	FY22	FY23	FY24	Grand Total
System Integration	**1.00**	**2.00**	**2.00**	**2.00**	**2.00**	**3.00**	**3.00**	**15.00**
6.4.6.4 System Integration	1.00	2.00	2.00	2.00	2.00	3.00	3.00	15.00
PA/Shaper	**2.73**	**2.43**	**2.80**	**2.00**	**2.00**	**-**	**-**	**11.96**
6.4.6.5 PA/Shaper	1.50	1.50	1.50	1.50	1.50	-	-	7.50
6.4.7.5 PA/Shaper	1.23	0.93	1.30	0.50	0.50	-	-	4.46
DOE Grand Total	**3.73**	**4.43**	**4.80**	**4.00**	**4.00**	**3.00**	**3.00**	**26.96**

DOE Cost and Effort (by Phase)

6.4 Liquid Argon DOE Total Cost by Phase (AYk$)								
Deliverable/Item/Phase	FY18	FY19	FY20	FY21	FY22	FY23	FY24	Grand Total
6.4.6 LAr_BNL	**687**	**900**	**979**	**892**	**914**	**727**	**747**	**5,845**
6.4.6.4 System Integration	**248**	**448**	**464**	**475**	**488**	**727**	**747**	**3,596**
Design	248	448	464	0	0	0	0	1,159
Prototype	0	0	0	475	488	0	0	963
Production	0	0	0	0	0	727	747	1,474
6.4.6.5 PA/Shaper	**439**	**452**	**515**	**417**	**426**	**0**	**0**	**2,249**
Design	439	0	0	0	0	0	0	439
Prototype	0	452	515	0	0	0	0	967
Production	0	0	0	417	426	0	0	843
6.4.7 LAr_Penn	**182**	**135**	**173**	**88**	**90**	**0**	**0**	**667**
6.4.7.5 PA/Shaper	**182**	**135**	**173**	**88**	**90**	**0**	**0**	**667**
Design	182	0	0	0	0	0	0	182
Prototype	0	135	173	0	0	0	0	308
Production	0	0	0	88	90	0	0	178
DOE Grand Total	**868**	**1,034**	**1,152**	**980**	**1,004**	**727**	**747**	**6,513**

System Integration

- WBS 6.4.x.4 covers "System Integration" task at BNL, which is part of DOE scope

- Work involved includes:

  - Frontend Crate System Test, performed to validate the FE system integration and overall performance before PRRs of the various FE crate boards (including FEB2)

  - Validation and final analog tests
  of 50% of the FEB2 boards

  - Integration and combined system
  test of FE and BE electronics

- The equivalent tests were
performed at BNL during the
original ATLAS construction
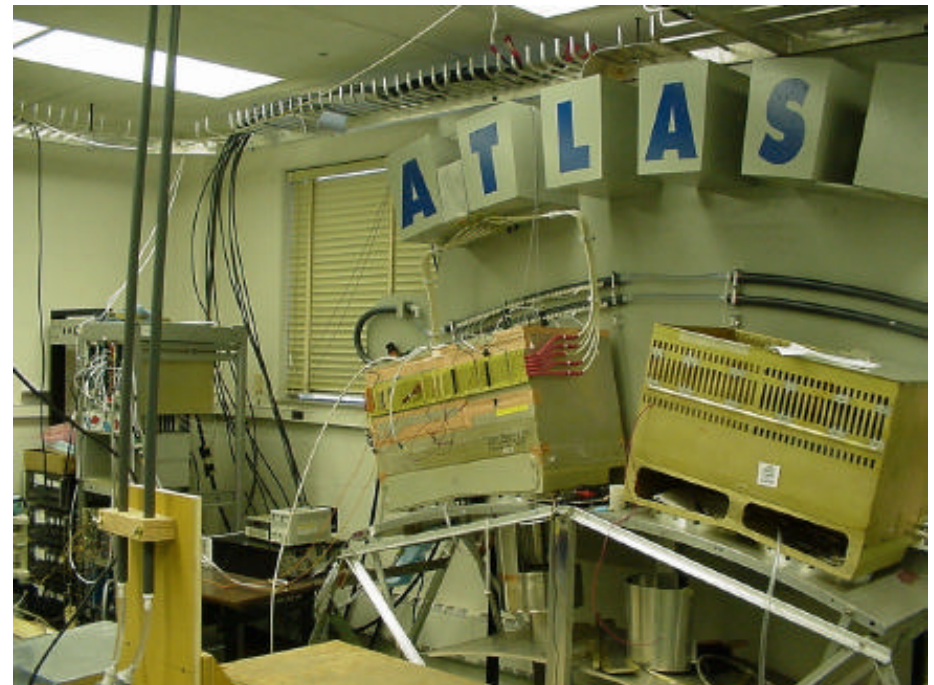
LAr HL-LHC Upgrade Motivation : Forward Region

- HL-LHC physics program (in particular, VBF Higgs production, VBS, …) places a premium on detector performance in the forward region

- At HL-LHC rates, existing FCAL will suffer degraded performance, due to space charge effects, time-dependent HV due to drops across HV resistors, …
  - Also, there are some concerns (being investigated) that there could be LAr boiling

- A number of options being considered:
  1. Replace FCAL with new sFCAL with thinner LAr gaps (to avoid space charge problems), which could have finer granularity for enhanced performance
  2. Place "miniFCAL" in front of existing FCAL, to absorb some of the energy
  3. Do "nothing" and live with degraded FCAL performance

- Also investigating placing a "4D" high-granularity timing detector (HGTD) in front of endcap cryostats, to help with pileup rejection, aid in triggering, improve EM response in forward region, …

sFCAL (WBS 6.4.x.6)

- A novel feature of ATLAS is LAr "rod-and-tube"-geometry forward calorimeter (FCAL), developed by U Arizona group
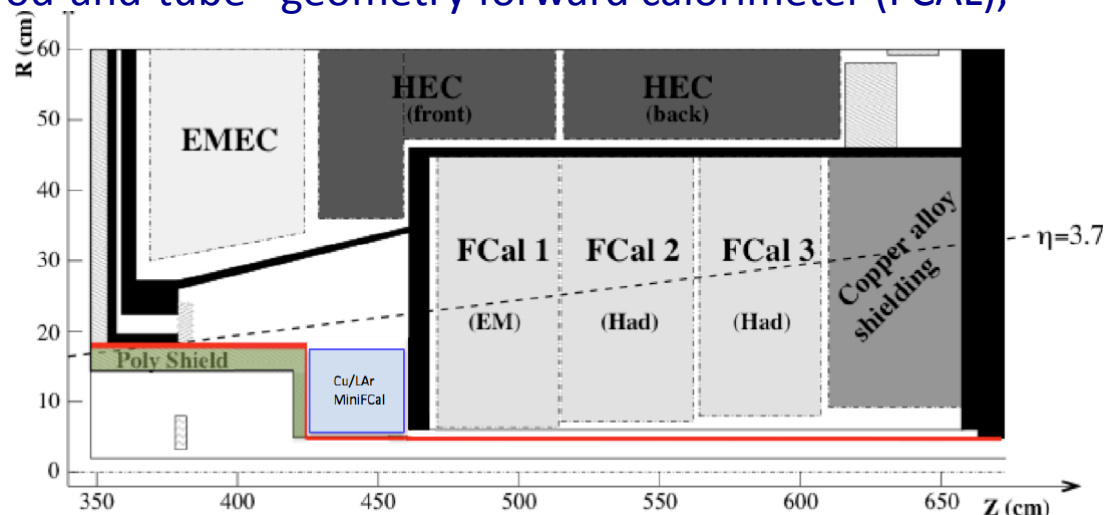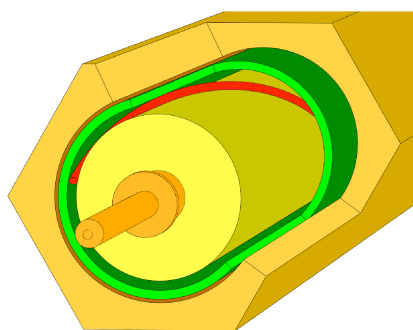
- New sFCAL with thinner gaps (down to 100 μm, instead of 270 – 500 μm) would avoid space charge and other problems in HL-LHC environment
  - sFCAL would also allow finer granularity, and therefore improved performance
  - As for current FCAL, U Arizona to produce sFCAL1 modules, as well as cold electronics

- sFCAL performance needs to be evaluated, and balanced against risks involved in opening cryostats (in pit) to replace FCAL
  - Other options include MiniFCAL in front of FCAL, or doing nothing
  - ATLAS decision about FCAL options planned to be made in June 2016
  - For now, sFCAL (WBS 6.4.x.6) is included in DOE "Scope Opportunity" (~ $5.4M)

High-Granularity Timing Detector HGTD (WBS 6.4.x.7)

- Possible new "4D" detector in front of EC cryostats
  - Δz = 60 mm detector; $|\eta|$ range of 2.4 – 4.1 (or even up to 5.0)

- Assuming multiple (eg. 4) layers of Si-based detectors (eg. LGADs developed by UCSC with some CMS collaborators)
  - Want time resolution of 30-50 ps and granularity of 1-100 mm^2
  - Could include absorber plates if also used as preshower
  - Synergies with option of Si/Cu miniFCAL (and also CMS HL-LHC)

- US groups and personnel are providing significant leadership of HGTD, with roles including:
  - Francesco Lanni, BNL (HGTD co-Convenor)
  - Abe Seiden, UCSC (co-Convenor of Detector System group)
  - Ariel Schwartzman, SLAC (co-Convenor of Software&Perf.group)

- Simulation program underway to investigate physics impact

- In parallel, proceeding with R&D on detectors, readout, …

- ATLAS decision whether to build HGTD planned for May 2017
  - Possible US HGTD contribution (WBS 6.4.x.7) included in DOE "Scope Opportunity" (~ $5.3M)
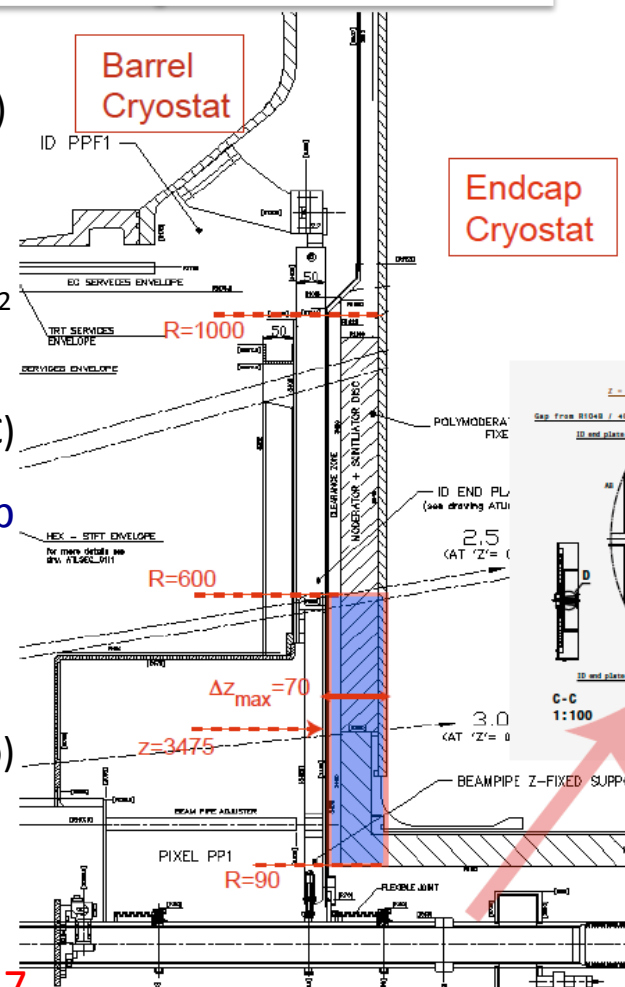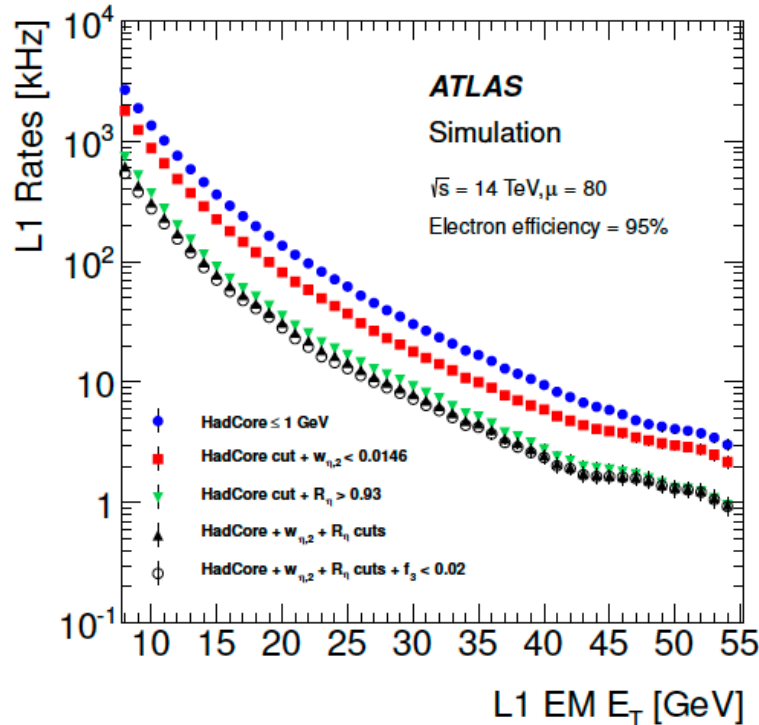
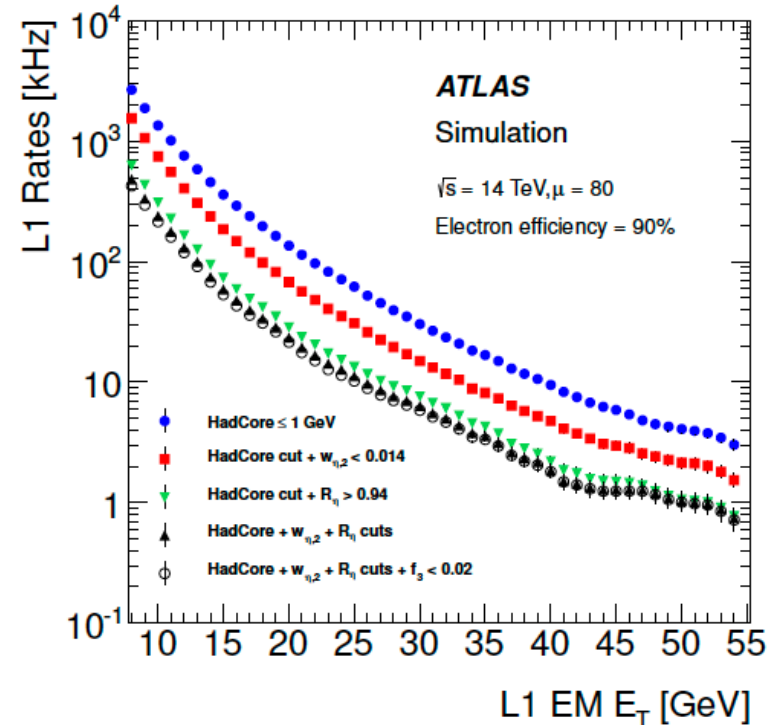**Table 26: Questions for Checking the Accuracy of Estimating Techniques**

Technique	Question
Analogy	▪ What heritage programs and scaling factors were used to create the analogy? ▪ Are the analogous data from reliable sources? ▪ Did technical experts validate the scaling factor? ▪ Can any unusual requirements invalidate the analogy? ▪ Are the parameters used to develop an analogous factor similar to the program being estimated? ▪ How were adjustments made to account for differences between existing and new systems? Were they logical, credible, and acceptable?
Data collection	▪ How old are the data? Are they still relevant to the new program? ▪ Is there enough knowledge about the data source to determine if it can be used to estimate accurate costs for the new program? ▪ Has a data scatter plot been developed to determine whether any outliers, relationships, and trends exist? ▪ Were descriptive statistics generated to describe the data, including the historical average, mean, standard deviation, and coefficient of variation? ▪ If data outliers were removed, did the data fall outside three standard deviations? ▪ Were comparisons made to historical data to show they were an anomaly? ▪ Were the data properly normalized so that comparisons and projections are valid? ▪ Were the cost data adjusted for inflation so that they could be described in like terms?
Engineering build-up	▪ Was each WBS cost element defined in enough detail to use this method correctly? ▪ Are data adequate to accurately estimate the cost of each WBS element? ▪ Did experienced experts help determine a reasonable cost estimate? ▪ Was the estimate based on specific quantities that would be ordered at one time, allowing for quantity discounts? ▪ Did the estimate account for contractor material handling overhead? ▪ Is there a definitive understanding of each WBS cost element's composition? ▪ Were labor rates based on auditable sources? Did they include all applicable overhead, general and administrative costs, and fees? Were they consistent with industry standards? ▪ Is a detailed and accurate materials and parts list available?
Expert opinion	▪ Do quantitative historical data back up the expert opinion? ▪ How did the estimate account for the possibility that bias influenced the results?

Phase I Example of Improving Trigger Rates via Finer Granularity

Figure 10. Trigger rates for $\mathcal{L} = 3 \times 10^{34}$ cm^{-2} s^{-1} as a function of E_T thresholds with optimized requirements on *HadCore*, $w_{\eta,2}$, R_η, and f_3. Subfigures (a) and (b) correspond to trigger efficiencies of 95% and 90%, respectively, for electrons from simulated $Z \rightarrow e^+e^-$ decays.
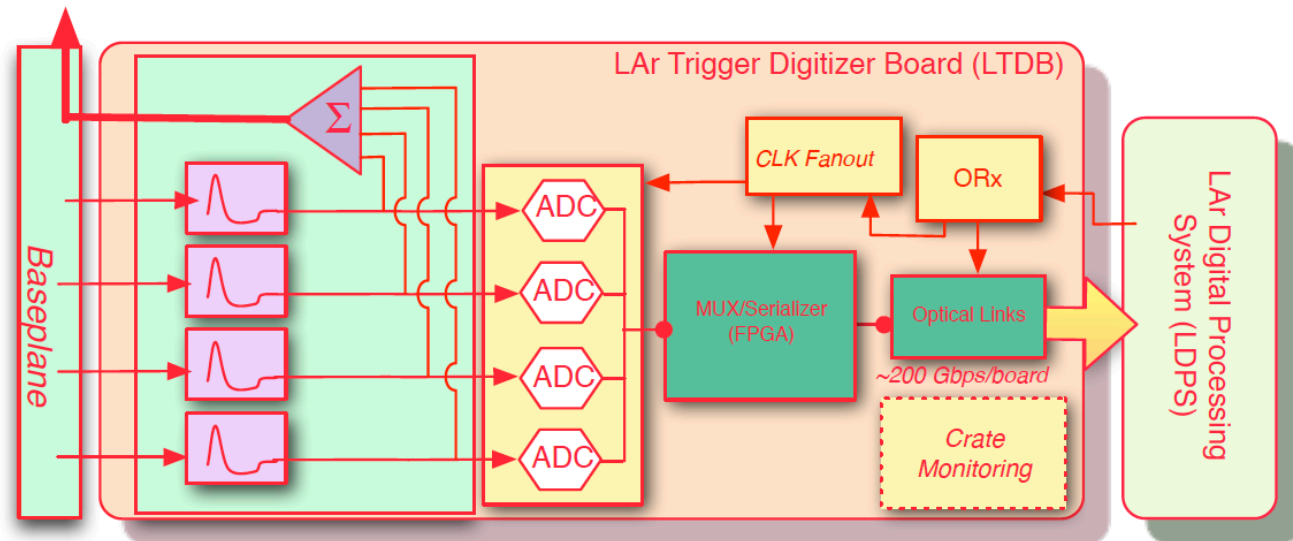
Phase I LAr Trigger Digitizer Board

Figure 29. Schematic block diagram of the proposed LAr Trigger Digitizer Board (LTDB).

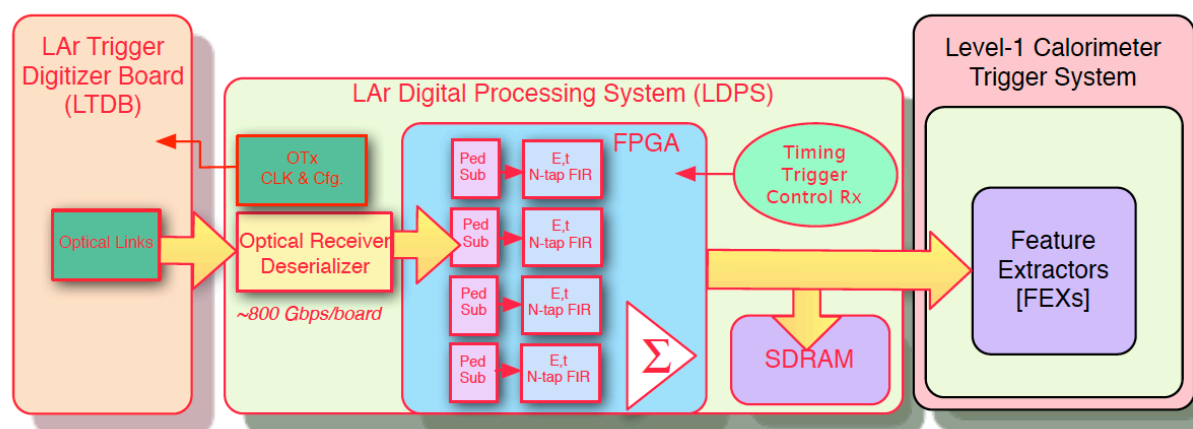# Phase I LAr Digital Processing System

Figure 48. Block diagram of the proposed LAr Digital Processing System (LDPS), which receives digital Super Cell data from the LTDBs of the upgraded FE system, reconstructs $E_{\mathrm{T}}^{\text{Super Cell}}$ (the transverse energy of each Super Cell), and transmits the results to the Level-1 Calorimeter Trigger System every 25 ns.